Understanding Radiation- and Hot Carrier-Induced Damage Processes in SiGe HBTs Using Mixed-Mode Electrical Stress

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***Abstract*—Using mixed-mode annealing to help evaluate the responses of modern bipolar transistors, we compare the damage processes associated with X-ray irradiation-induced and hot carrier-induced damage in SiGe HBTs. Stress and radiation measurements indicate that the by-products of both X-ray irradiation-induced and hot carrier-induced trap reactions are identical. We use calculations to better understand the operative damage mechanisms, and find that a hydrogen reaction-diffusion model can predict the observed characteristics of our measurements. Calculations indicate that the transport of hydrogen molecules inside the emitter-base oxides determines the trap generation and recovery processes.**

***Index Terms*—Mixed-mode anneal, mixed-mode stress, reaction-diffusion model, SiGe, SiGe HBTs, silicon-germanium, thermal anneal, X-ray irradiation.**

I. Introduction

As SiGe technology becomes increasingly adopted for a wide variety of high-performance, mixed-signal circuits, better understanding and modeling of the underlying SiGe HBT reliability in its diverse application contexts are required. Current reliability lifetime models for hot carrier degradation associated with industry-standard electrical "burn-in" protocols in SiGe HBTs are purely empirical, and the exact damage mechanisms remain poorly understood. For instance, interface traps (dangling Si bonds that result from the breaking of Si-H bonds) are generally assumed to result from electrically-induced hot carrier stress but the specifics of the trap formation process in SiGe HBTs have not been adequately addressed. Furthermore, current TCAD simulation tools base their models of trap generation in SiGe HBTs on purely CMOS stress data, which may or may not be applicable to advanced SiGe HBTs (or even to conventional Si BJTs).

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Due to the scaling-induced voltage limitations of SiGe HBTs imposed in the quest for higher frequencies, designing robust circuits has become a challenge; it becomes even more complex to assess their reliability, given the various topologies which require very different bias conditions. For example, the cascode circuit topology has become a preferred design approach for SiGe amplifiers, in which the cascode HBT sees zero impedance at the base and high impedance at the emitter. In the case of mixed-signal systems, when analog circuits are interfaced to digital circuits, the voltage and current characteristics become highly unpredictable, and thus devices can be simultaneously and dynamically subjected to both high voltage and high current. The traditional bipolar electrical stresses, namely, reverse-EB stress [1] and the high-current stress [2], can not be applied to these aggressive stress conditions. Mixed-mode stress was created to tackle these challenges [3]. Later, mixed-mode stress was expanded to very low currents and voltages as well the range in between [4]. Contrary to the naïve assumption of a single operative damage mechanism, several have been in fact observed, and the conditions at which these mechanisms occur are dependent upon the geometry, voltage, current, and temperature of the SiGe technology in question [4].

As discussed in [4], hot-carrier-induced damage in advanced SiGe HBTs can be removed when the damaged devices are subsequently subjected to additional electrical stress under very specific bias conditions, and this process was termed "mixed-mode annealing." In our present work, we show that mixed-mode annealing can also remove radiation-induced damage. By employing mixed-mode annealing studies in SiGe HBTs, both hot-carrier and radiation-induced damage can be removed at approximately the same effective junction temperature, and have approximately the same time dependence. In addition, the resultant ideality factors of the induced excess base current for these two damage mechanisms have been shown to be nearly identical. The similarity of the annealing behavior for these two very different types of trap introduction processes suggests that radiation-induced and hot-carrier-induced damage in SiGe HBTs are the result of one common damage mechanism, and which we believe can be adequately described by existing trap formation and annealing models (e.g., [5]).

Our present work also provides a theoretical understanding of trap generation and recovery in SiGe HBTs that is relevant to both hot carrier stress and radiation. We present calculations

based on a hydrogen reaction-diffusion model to better understand the power law time dependence observed during electrical stress, the logarithmic time dependence observed in electrical stress and radiation damage, and the critical role hydrogen molecules play in the trap reaction kinetics. Given the similarities observed between electrical stress and radiation damage, and employing the first-principles' simulations developed in [5], we discuss the implications for device reliability.

II. Devices and Test Conditions

Our experiments include electrical stress and irradiation of two different commercially-available SiGe technology nodes. SiGe HBT A is a 0.5 μm lithography technology with peak $\mathrm{f_T} = 50$ GHz and $\mathrm{BV_{ceo}} = 3.3$ V [6] and SiGe HBT B is a 130 nm lithography technology with a peak $\mathrm{f_T} = 200$ GHz and $\mathrm{BV_{ceo}} = 1.8$ V [7]. Two electrical stress techniques, both conventional reverse-bias EB and "mixed-mode" stress, were employed on multiple samples of SiGe HBTs A and SiGe HBT B, with consistent results. Two configuration of reverse-EB stress were used, the open-collector (OC) and forward-collector (FC) mode. In OC mode, EB junction is reversed biased with collector open, whereas in the FC mode the collector-base junction is forward-biased to inject electrons into the reversed-biased EB junction [1].

The standard way to mixed-mode stress a transistor is to ground the base, reverse-bias the CB junction, and force a negative current at the emitter. Thus, the device is in forward-bias mode under high current and voltage levels. In this manner, the number of carriers injected into the high CB electric field is very well controlled. Although this approach may seem a rather unlikely configuration, it eliminates the problem of thermal runaway, as in the case of a forced base- and collector-voltage configuration [8]. Another way to assess mixed-mode damage is called the mixed-mode current sweep, which will be described in a later section.

For X-ray irradiation experiments, the SiGe HBTs were wire-bonded into 28-pin DIP packages. Ionizing radiation was applied at room temperature using 10 keV X-rays, at a dose rate of 540 rad(SiO_2)/s, to a maximum total dose of 5.4 Mrad(SiO_2). Some devices were irradiated with all pins grounded, while others were irradiated under forward-active bias. Devices were pulled from the beam, measured immediately after a given total dose, and then re-inserted into the beam to reach the next total dose point. Post-irradiation measurements were also made after approximately four weeks to check for spontaneous annealing. The bias conditions applied during irradiation did not affect the observed damage significantly.

Thermal experiments were also performed. Wafers were inserted into the chamber of an AET addax RX Rapid Thermal Annealer, which can accurately control the annealing temperature, duration, and the ambient gas mixture inside the chamber. Device thermal resistance used in this work was extracted and reported in [4] by correlating the junction temperature with dissipated power [9].

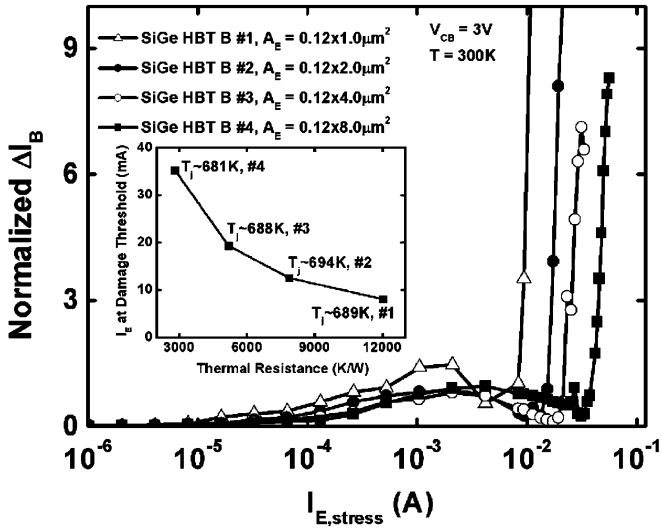

Fig. 1. Damage spectrum for mixed-mode stress, with varying transistor geometries. During stress, $V_{\mathrm{CB}} = 3$ V, and base current was measured at $V_{\mathrm{BE}} = 0.6$ V.

III. Experimental Results

We have used a recently developed electrical stress methodology called "mixed-mode current sweep" to identify the various operative damage mechanisms [4]. Essentially, a device is stressed at increasingly higher emitter current $I_{E,\mathrm{stress}}$ (at fixed V_{CB} and stress time intervals ranging from 10 to 250 s) until it degrades and eventually fails. This electrical stress method allows one to obtain quickly the general damage response (spectrum) over a very wide range of stress conditions. Typical current sweeps for SiGe HBT B of varying geometry are shown in Fig. 1, which plots normalized change in base current ($\Delta I_B = (I_{B,\mathrm{post}} - I_{B,\mathrm{pre}})/I_{B,\mathrm{pre}}$) versus increasing $I_{E,stress}$. The stress V_{CB} was fixed at 3 V, and excess base current was measured at $V_{\mathrm{BE}} = 0.6$ V. Stress-induced excess I_B can be observed at very low (circuit relevant) values of $I_{E,\mathrm{stress}}$. We call this stress region "low-current mixed-mode stress." Interestingly, however, the accumulated damage begins to decrease after $I_{E,\mathrm{stress}}$ increases beyond some level. We call this damage-decrease region "mixed-mode annealing." At a particular $I_{E,\mathrm{stress}}$ threshold, damage starts to rapidly increase again. We call this region "high-current mixed-mode stress." This latter region is consistent with our earlier studies in mixed-mode stress [3]. The damage threshold in which high-current mixed-mode stress is initiated varies with the thermal resistance of the device, as shown in the inset of Fig. 1. However, the junction temperature $T_J (T_J \approx \mathrm{V_{CE}} \times \mathrm{I_{E,stress}} \times \mathrm{R_{th}} + T_{\mathrm{amb}}$ [9]) at the damage threshold is the same for all of these devices ($\sim$ 690 K), suggesting that temperature plays a strong role in high-current mixed-mode stress. The base leakage currents in this work are all plotted at $V_{\mathrm{BE}} = 0.6$ V, and details of the stress and radiation experiments are listed in the figures.

Results of thermal annealing experiments are shown in Fig. 2. First, devices were low-current, mixed-mode stressed for 1000 s (stressed at $V_{\mathrm{CB}} = 3$ V and $J_C = 10$ mA/μm ^{2}), and then thermal-annealed (within the rapid thermal annealer

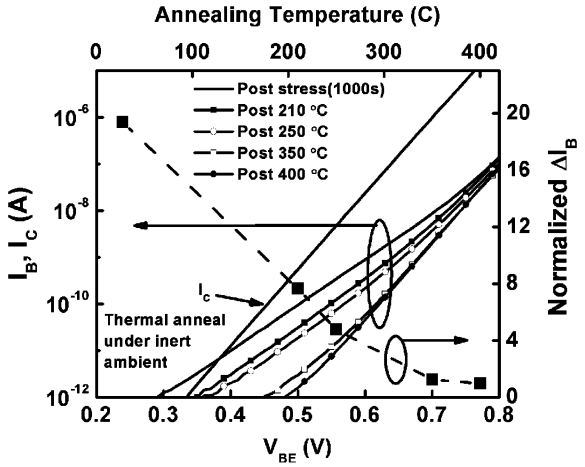

Fig. 2. Gummel characteristics of the thermal annealing experiments. The devices were first low-current mixed-mode stressed.

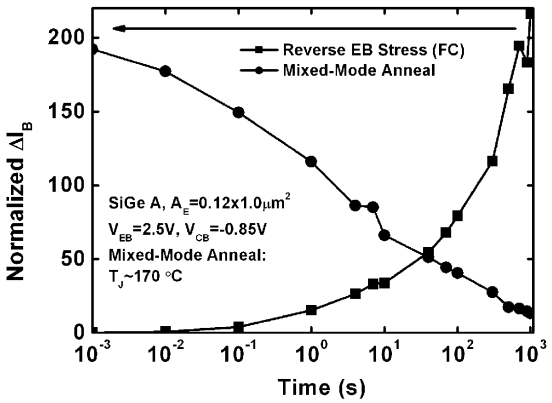

Fig. 3. Normalized excess base current as the device was reverse-EB stressed (FC mode) and then mixed-mode annealed.

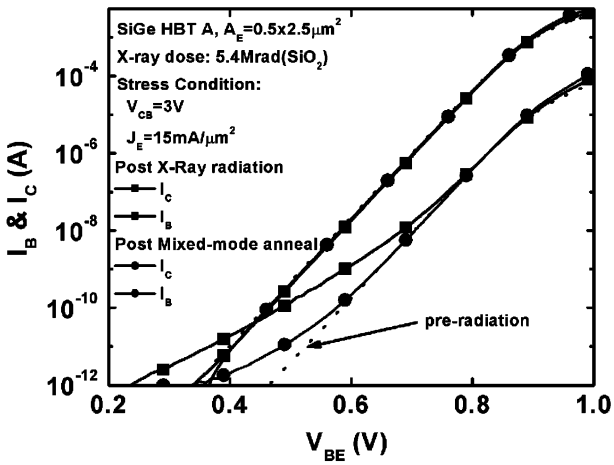

Fig. 4. Measurements of X-ray irradiation damage followed by mixed-mode annealing.

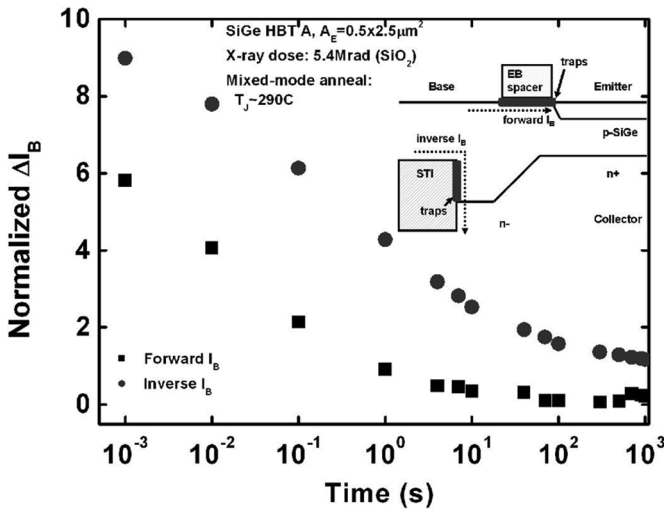

Fig. 5. Excess base current normalized by pre-stress I_B during mixed-mode anneal.

and unbiased) in nitrogen ambient for 15 minutes. As shown in Fig. 2, much of the damage is removed at $T_{\rm oven} = 210\,^{\circ}$C, and more damage is removed with increasing anneal temperature. Given that temperature alone can anneal the stress damage, self-heating due to high-current stress conditions should also initiate an annealing process. Furthermore, mixed-mode annealing can remove not only low-current mixed-mode stress, but also reverse-bias EB stress. This was confirmed in our time-dependent experiments. An example of this stress procedure is shown in Fig. 3. The device is reverse-EB (in FC mode [1]) stressed for 1000 s and then immediately subjected to mixed-mode anneal at $T_J \sim 170\,^{\circ}$C for 1000 s. I_B at $V_{\rm BE} =$ 0.6 V increased to more than 200× its original value; after 1000 s of mixed-mode anneal the excess current recovers by a factor of 16.

Mixed-mode annealing was also applied to SiGe HBT A devices that have been X-ray irradiated, as shown in Fig. 4. After X-ray irradiation an excess base current was observed, as expected, but this current was dramatically reduced after mixed-mode anneal. Fig. 5 shows the excess base current normalized by pre-stress I_B during the annealing process. The normalized forward ΔI_B is reduced by a factor of 25, while the normalized inverse mode (swapping the emitter and collector terminals) ΔI_B decreased by a factor of 8. SiGe HBT B devices were also irradiated with X-rays, and they were similarly mixed-mode annealed. Forward and inverse mode ΔI_B normalized by pre-stress I_B data are shown in Figs. 6 and 7. The annealing rate is approximately the same for the different anneal temperatures. After some fixed total time, the annealing saturates, and sometimes additional damage can be introduced into the device.

Fig. 8 shows the time dependence of the mixed-mode annealing process for various applied stress conditions. Excess base current data are now normalized by the maximum ΔI_B. Observe that the various types of damage (via irradiation or electrical stress) are all annealed at approximately the same rate. Fig. 9 shows the time dependence of the various types of electrical stress. The time dependence is nearly the same, following a power law response of $\Delta I_B = At^{0.35}$, where t is stress time and A is a constant of proportionality.

To better understand the operative annealing process, devices were cyclically damaged and annealed, over many repetitions (Fig. 10). The device was first low-current, mixed-mode stressed for 1000 s at $J_{E,\rm str} = 2$ mA/μm^2, and then mixed-mode an-

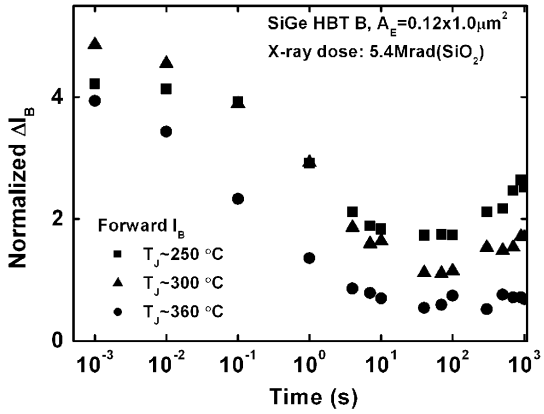

Fig. 6. Excess base current normalized by pre-stress I_B (in forward mode) of mixed-mode annealing using different junction temperatures.

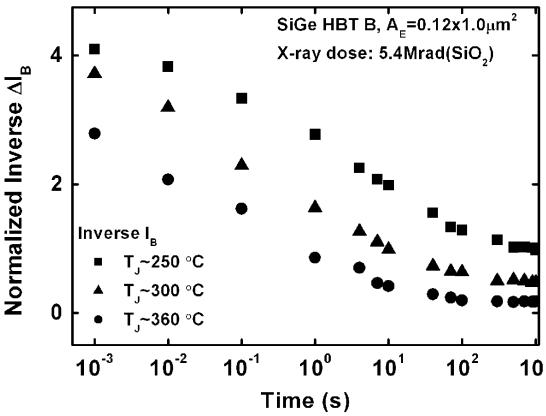

Fig. 7. Excess base current normalized by pre-stress I_B in inverse mode of mixed-mode annealing using different junction temperatures.

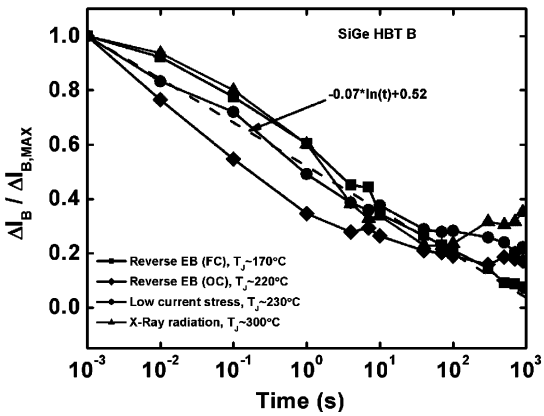

Fig. 8. Comparison of annealing rate of various types of damage. Excess base current is normalized by the maximum excess base current. Reverse-EB FC mode indicates forward biasing base-collector voltage during stress, and reverse-EB OC mode indicates opening the collector during stress.

nealed for an additional 1000 s, and then the process was repeated for 48 cycles. In total, the device was stressed and annealed for over 26 hours. Fig. 10 shows the evolution of the excess base current at $V_{\rm BE} = 0.6$ V after each cycle of stress and

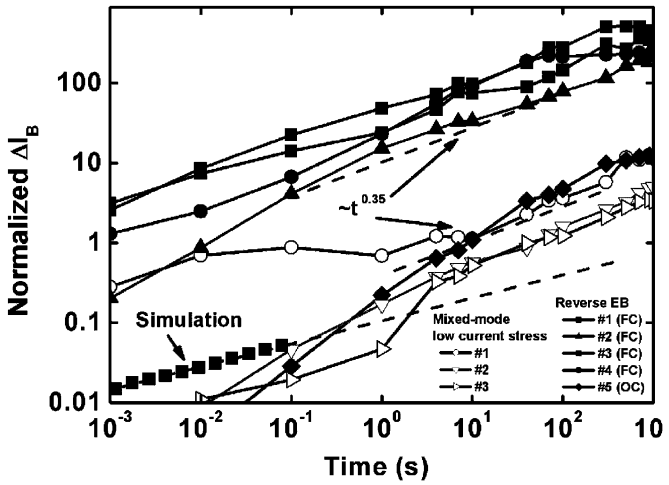

Fig. 9. Time dependence of normalized excess base current, for various types of damage. Simulation of the power law time dependence is also shown. The generation rate k_g was 0.1/s, and recovery rate k_r was 10^{-7} cm^3/s. The diffusion constant used was 0.01 μm^2/s.

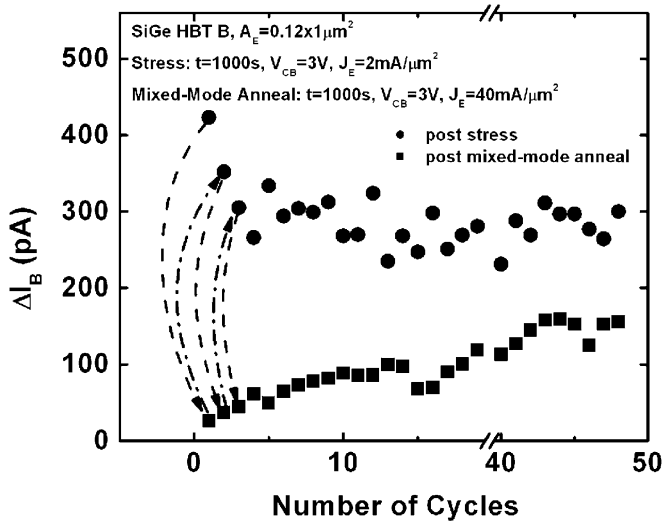

Fig. 10. Excess base current as the devices were cyclically stressed and annealed.

anneal. The base current after each anneal increases slightly, indicating that the annealing removes fewer traps with each increasing cycle.

The ideality factor of the excess base current was extracted during all of the experiments. The mean and variance (extracted from a total of 900 measurements) of the ideality factor for the various methods of electrical stress are approximately the same, with a mean value of 1.77 and standard deviation of 0.12. The ideality factor extracted from X-ray irradiation (30 measurements) had a mean value of 1.78 and a standard deviation of 0.13. Shown in Fig. 11 is a comparison of base leakage current observed at low forward EB voltages, and it is clear that radiation and electrical stress produce about the same ideality factor of $\sim$1.8.

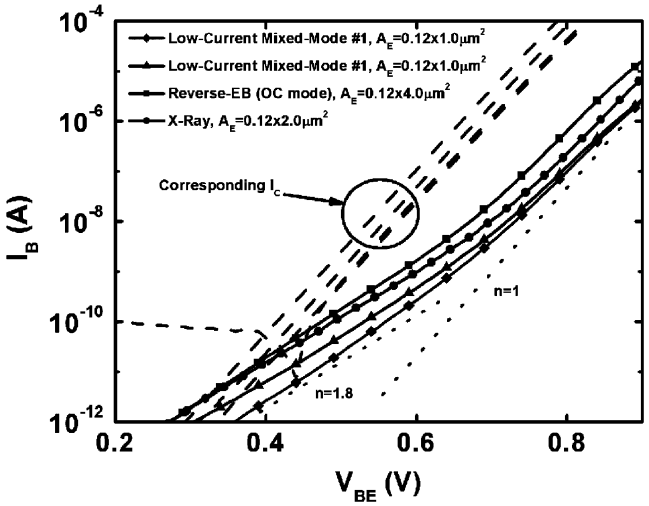

Fig. 11. Comparison of base current leakage in SiGe HBT B after X-ray irradiation and electrical stress. The ideality factors of the base leakage current were all around 1.8.

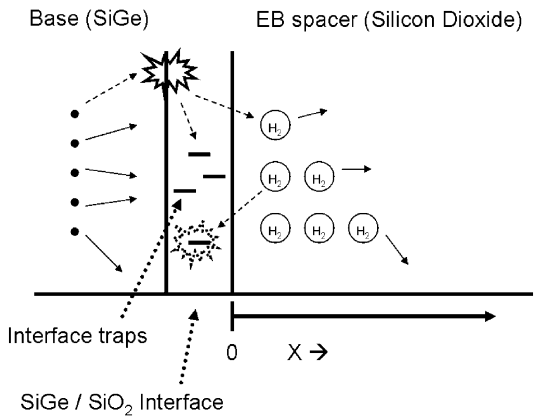

Fig. 12. Diagram of the reaction-diffusion model used in the calculations. Hot carriers break bonds at the interface to create traps and H_2. H_2 at the interface can participate in the recovery process to remove traps.

IV. Calculation

The proposed scenario of interface trap generation and recovery is depicted in Fig. 12. Hot carriers near the interface result in broken Si-H bonds, liberation of H atoms, and creation of interface traps and H_2 molecules [10], [11]. Since H_2 molecules are slow to diffuse away from the interface, some will stay near the interface and participate in the recovery process [12]–[14], in which interface traps are passivated. Interface trap generation and recovery are modeled as follows [5]. At the interface, the change in trap concentration with respect to time is given by

$$\frac{dN_{\rm IT}}{dt} = k_g(N_0 - N_{\rm IT}) - k_r N_{\rm IT} H_0. \tag{1}$$

Here $N_{\rm IT}$ is the areal interface-trap density, N_0 is the areal density of initial Si-H bonds, k_g and k_r are generation and recovery rates, and H_0 is the volumetric H_2 concentration at the interface; one H_2 molecule can depassivate two traps. The hydrogen molecules generated due to stress can not easily diffuse into silicon; however, they can diffuse into the oxide [5]. The hydrogen molecules will move away from the interface in a similar manner to that governed by the 1-D heat equation

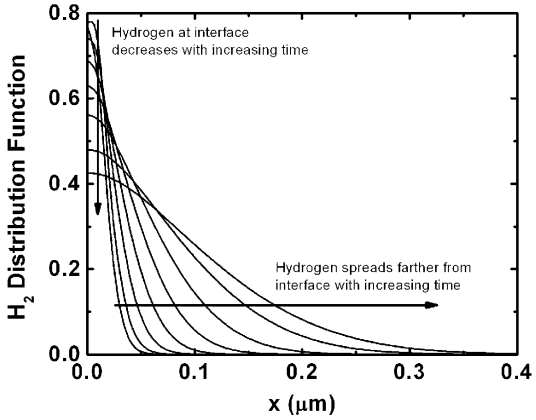

Fig. 13. Distribution of calculated H_2 during trap generation, with increasing stress time.

$$\frac{dH_2(x,t)}{dt} = k\frac{d^2H_2(x,t)}{dx^2} \tag{2}$$

where k is the diffusion constant of H_2 in the oxide, and $H_2(x)$ is the distribution of the H_2 concentration in the EB spacer oxide. Note that the diffusivity is temperature dependent.

Equations (1) and (2) are simultaneously solved in MATLAB's Partial Differential Equation Toolbox. The EB spacer is modeled as a 1 μm thick oxide, and the simulation time is made up of 50 logarithmically spaced time-steps, from 1 ms to 1 s. For the annealing process, a much higher value of k was used than that of the trap generation process. This is because the diffusion constant is thermally-activated, and thus will increase when the internal temperature of the EB spacer is elevated. During thermal anneal, the EB spacer is at the annealing temperature. During mixed-mode anneal, the temperature of the EB spacer is not known. However, the temperature near the interface typically must be at least ~80–100 °C for interface traps to be removed [15], [16], and may well be as high locally as ~150 °C [5].

The calculation results of this trap generation process are shown in Fig. 9, yielding a power law exponent of ~0.3, which is reasonably close to the value of 0.35 obtained from measurements. It was predicted in [17] that, if the trap concentration changes slowly with time, then a power law of ~0.25 should result. At first glance this power law behavior may appear to be impossible to achieve using (1). According to (1), the trap generation rate stays nearly constant ($N_0 \gg N_{\rm IT}$), whereas the trap recovery rate is nonlinear. If both $N_{\rm IT}$ and H_0 increase with increasing stress time, then the recovery rate would quickly become larger than the trap generation rate. However, since the diffusion of hydrogen is much slower than trap generation (here, $k = 0.01$ μm^2/s), it becomes the dominating factor [17], and this can be observed in the evolution of hydrogen molecule profiles during stress (Fig. 13), in which the hydrogen concentration at the interface actually *decreases* as the trap generation progresses and the hydrogen diffuses away from the interface.

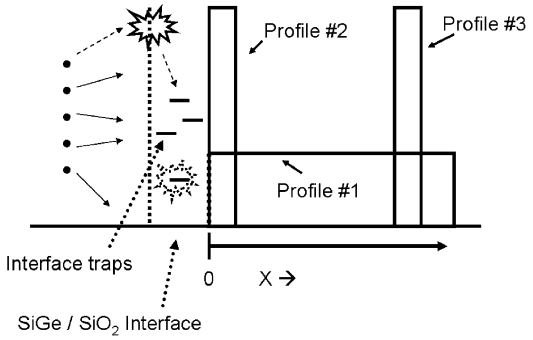

Fig. 14. Hydrogen profiles used in the calculations to probe the effects of the shape of the H_2 profile on annealing.

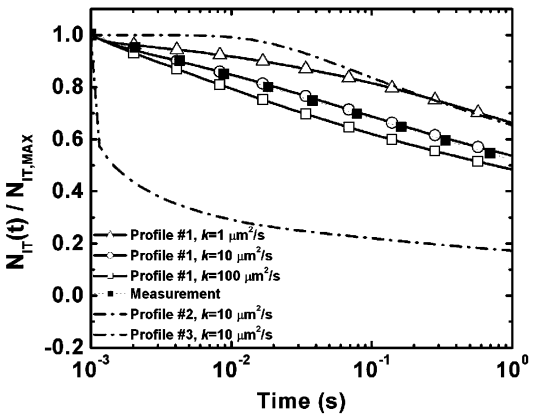

Fig. 15. Calculation of annealing with respect to time. Different H_2 profiles and diffusion constants were used.

Therefore, the decreasing H_0 offsets the increasing $N_{\rm IT}$ concentration, producing a stable $t^{0.3}$ curve.

Various scenarios of interface trap recovery during anneal were calculated. Three different hydrogen profiles were used, as shown in Fig. 14. How the annealing process is affected by the different hydrogen profiles is essential to understanding the annealing mechanism. First, a flat hydrogen molecule profile (#1) was used, and the diffusion constant (k) was varied across a large range. As shown in Fig. 15, when k = 10 μm^2/s, the annealing characteristics nearly overlay the measurement results. As the diffusion constant was increased ($k = 100$ μm^2/s), the annealing process was only slightly accelerated, whereas decreasing the diffusion constant ($k = 1$ μm^2/s) slowed down the anneal process. This is because higher diffusion constant will cause more hydrogen molecules to propagate to the interface, and thus more traps will be annealed. However, at a certain point, increasing diffusivity no longer has any effect, because ultimately the annealing process is limited by the total available hydrogen.

Calculation results of the other two hydrogen profiles are also shown in Fig. 15. For profile #2, the trap recovery rate was extraordinarily high in the beginning, but soon reverted back to the typical logarithmic time dependence. For profile #3, the trap recovery rate was nearly zero in the beginning; however, after 0.01 s, the logarithmic time dependence again appeared. These two hydrogen profiles, due to their large initial diffusion gradients, quickly spread out to move farther and farther away

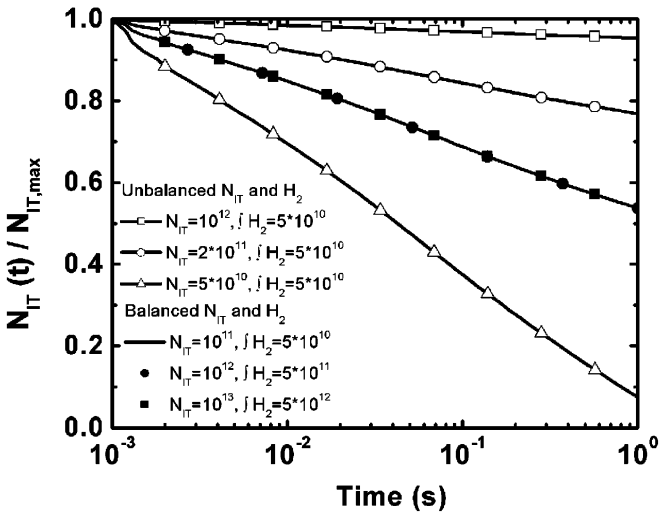

Fig. 16. Calculation of trap anneal with respect to time. Different concentrations were used to better understand the annealing rate. $N_{\rm IT}$ means the total number of interface traps, and $\int H_2$ means the total number of hydrogen molecules, integrated over the entire oxide.

from their original locations. Since the hydrogen concentration of profile #2 was largest at the beginning, the initial annealing rate was very high. As it spreads out, it is transformed into a flatter shape, much like profile #1, thus reverting back to the logarithmic rate. As for profile #3, it took some time for the hydrogen to reach the interface (since it was farther away), but by that time the profile again becomes similar to profile #1, and thus the same logarithmic rate is again observed.

During stress, it is possible that some hydrogen diffuses so far away from the interface that it will never travel back. In that case, there will be more interface traps than there are hydrogen molecules during the anneal process. In addition, it is possible that there was a large concentration of H_2 already in the EB spacer oxide, and in this case there will be more hydrogen than interface traps. Calculation results of these two scenarios are shown in Fig. 16. Profile #1 was used for these calculations, all using $k = 10$ μm^2/s for the diffusion constant. When there is more hydrogen than interface traps ($N_{\rm IT} = 5 * 10^{10}$ and $\int H_2 = 5 * 10^{10}$, which is 10^{11} H atoms), the annealing process is dramatically faster than when the hydrogen concentration balances that of the interface traps (i.e., $N_{\rm IT} = 10^{11}$ and $\int H_2 = 5 * 10^{10}$, which is 10^{11} H atoms). When there are more interface traps than available hydrogen (i.e., $N_{\rm IT} = 10^{12}$ and $\int H_2 = 5 * 10^{10}$), the annealing process dramatically decreases. This shows that the total concentration of H_2 ultimately determines the annealing rate. Since the balanced condition (shown in Fig. 16) overlays with measurements, this indicates that nearly all of the H_2 created during trap generation will participate in the annealing process.

V. Discussion

Significant effort has been focused on developing a better understanding of interface-trap formation, using radiation damage response as a powerful tool. One of the most widely accepted models of this trap formation mechanism is McLean's two-stage model [18], as also investigated extensively in poly-crystalline

Si devices by Saks and Brown [19]. Incident radiation produces electron/hole pairs, which in turn produce protons (H+), and then the protons propagate to the SiO_2/Si interface to produce interface traps. Recent work has examined: the effects of gate oxide electric field on trap generation rate [19], [20]; the effects of temperature on trap generation and the motion of protons near the device interface [5]; and a comparison of X-ray irradiation and hot-carrier induced stress, concluding that radiation-induced and hot-carrier-induced damage produce differing junction ideality factors [21]. Reference [22] reported experiments of hot-carrier stress and X-ray irradiation on multiple wafer lots, and found no correlation between the two types of damage.

In the work reported by Kosier *et al.* in [21], during irradiation, positive trapped charge is created in the oxide (N_{ox}), changing the surface potential near the emitter-base depletion region, and leading to a change in the excess base current, usually exhibiting an ideality factor much less than 2. When the trap charges were removed, ideality factor returns to 1.8, close to the ideal case of 2. Since the SiGe HBTs used in the present work have a very highly doped base, the effects of N_{ox} are dramatically reduced compared to those found in [21]. In other words trapped charges may exist but its effect on ideality factor is unobservable. This was confirmed from the extracted ideality factor data ($\sim$1.8), indicating that X-ray irradiation damage results mainly from EB interface traps.

We believe that the damage processes induced by X-ray irradiation and electrical stress in these devices are similar, for two reasons. First, the excess base current is due to SRH recombination, because the ideality factor is close to 2, for both damage types. Second, the rate of annealing and the temperature threshold to initiate annealing are approximately the same for various types of electrical stresses and X-ray irradiation.

A model based on first-principles molecular dynamics simulations was recently proposed in [5]. When trap generation dominates, as is the case when radiation-induced protons travel to the interface, Si-H bonds are depassivated, producing a silicon dangling bond and an H_2 molecule. At $\sim$150 °C, trap recovery dominates, in which H_2 passivates the dangling bonds to reform the Si-H bonds. Even though most of the annealing done in the present work likely occurs at 150 °C, current sweeps shown in Figs. 1 and 3 indicate that the annealing process actually begins at a lower temperature, approximately 130 °C. The similarity of the anneal temperature, together with the fact that the both are dealing with a trap at midgap, leads us to believe that the model described in [5] is applicable to our case.

Whereas Rashkeev *et al.* [5] used Monte Carlo techniques and a master equation to study the kinetics of the trap reaction with respect to temperature and the role of the various hydrogen species, in the present work we used a heat equation to better understand the time dependence of trap reaction, mainly through modeling the hydrogen-molecule transport inside the oxide. Based on work in [5] that the kinetics of the trap formation can be described using the reaction-diffusion model, we have proceeded to implement such a model in Matlab. The power law of $\sim$0.35 can indeed be simulated, as long as trap generation is dominated by the diffusion of hydrogen. The logarithmic annealing characteristics can also be predicted. The annealing process can deviate from this if the hydrogen profile is non-uniform, or the trap density is unbalanced with the available hydrogen molecule, or the diffusion constant is changed. For Figs. 6 through 8, indeed some variation from the logarithmic dependence can be observed, especially at lower annealing temperatures. Using the same annealing temperature (either using thermal or mixed-mode anneal), the annealing characteristics can be different, which may be explained through the possible non-uniformity of the hydrogen profile.

Our calculations may also be able to explain why annealing following irradiation, which was performed long after the radiation experiment, still has the same annealing characteristics as those of hot carrier stress. During the trap generation process, H_2 diffuses very slowly into the oxide, and it is possible that it remains very close to the interface, even after a long period of time. As thermal or mixed-mode annealing begins, the hydrogen profile should quickly diffuse outward, transforming from a near delta function to a flat distribution. Thus, by the time of the mixed-mode annealing experiment, even if the hydrogen profile during radiation is different than that of electrical stress (due to the long periods of time between damage and anneal for radiation), within a very short time the anneal process should flatten both enough to become similar to that of profile #1, again exhibiting the logarithmic time dependence.

With respect to device reliability, our calculations imply that trap generation should be slower at lower ambient temperature, and faster at higher ambient temperature, because the diffusion constant of H_2 depends on the ambient temperature. This is supported by the measurement results of [23], in which SiGe HBT A and B were irradiated at both room and cryogenic temperatures. For SiGe HBT A, the results are very clear; both forward and inverse mode excess base currents were much larger when irradiated at room temperature than when irradiated at 77 K. As for SiGe HBT B, the excess base current when irradiated at 300 K was slightly higher than when irradiated at 77 K. The differences between the two technologies may be understood by noting that the SiGe HBT A device used in [23] had an emitter perimeter larger than that of the SiGe HBT B devices, and due to the progressive scaling introduced to SiGe HBT B, the EB spacer oxide in SiGe HBT A is about fives times larger than that of SiGe HBT B (calculated from the layout of the devices). If the oxide is many times larger, then many more traps would be created at 300 than at 77 K. Thus, the effects of ambient temperature during irradiation should be much more noticeable for SiGe HBT A, which may account for the differences observed in the two technologies.

VI. Conclusion

We have investigated the damage mechanisms underlying X-ray irradiation and hot-carrier electrical stress in high-performance SiGe HBTs. Excess base current was observed when devices were exposed to large doses of radiation, and similar excess base current was also observed for various types of electrical stress, including reverse-EB and mixed-mode stress. Various means to damage the device produced almost the same excess base current; namely, they all exhibited ideality factors near 1.8. Mixed-mode annealing, in which the junction temperature was elevated to above $\sim$150 °C due to self-heating,

was observed to remove both electrical stress and X-ray irradiation damage. The temperature that trap annealing initiates, and the annealing rate for the various types of damage, were identical, suggesting that the two damage mechanisms, electrical stress and radiation, produced the same effects; namely, in both damage mechanisms, a trap near midgap and a H_2 molecule were generated at the interface. Using a hydrogen reaction-diffusion model, the time-dependent characteristics of trap generation and recovery were reproduced through calculation, and it was found that the transport and distribution of H_2 play an important role.

REFERENCES

[1] U. Gogineni, J. D. Cressler, G. Niu, and D. L. Harame, "Hot electron and hot hole degradation of UHV/CVD SiGe HBT's," *IEEE Trans. Electron Devices*, vol. 47, no. 7, pp. 1440–1448, Jul. 2000.

[2] J. S. Rieh, K. M. Watson, F. Guarin, Z. Yang, P. Wang, A. J. Joseph, G. Freeman, and S. Subbanna, "Reliability of high-speed SiGe heterojunction bipolar transistors under very high forward current density," *IEEE Trans. Device Mater. Reliab.*, vol. 3, no. 2, pp. 31–38, Jun. 2003.

[3] C. Zhu, Q. Liang, R. A. Al-Huq, J. D. Cressler, Y. Lu, T. Chen, A. J. Joseph, and G. Niu, "Damage mechanisms in impact-ionization-induced mixed-mode reliability degradation of SiGe HBTs," *IEEE Trans. Device Mater. Reliab.*, vol. 5, no. 1, pp. 142–9, Mar. 2005.

[4] P. Cheng, C. Zhu, A. Appaswamy, and J. D. Cressler, "A new current sweep method for assessing the mixed-mode damage spectrum of SiGe HBTs," *IEEE Trans. Device Mater. Reliab.*, vol. 7, no. 3, pp. 479–487, Sep. 2007.

[5] S. N. Rashkeev, D. M. Fleetwood, R. D. Schrimpf, and S. T. Pantelides, "Effects of hydrogen motion on interface trap formation and annealing," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3158–3165, Dec. 2004.

[6] D. L. Harame, D. C. Ahlgren, D. D. Coolbaugh, J. S. Dunn, G. G. Freeman, J. D. Gillis, R. A. Groves, G. N. Hendersen, R. A. Johnson, A. J. Joseph, S. Subbanna, A. M. Victor, K. M. Watson, C. S. Webster, and P. J. Zampardi, "Current status and future trends of SiGe BiCMOS technology," *IEEE Trans. Electron Devices*, vol. 48, no. 11, pp. 2575–2594, Nov. 2001.

[7] B. Jagannathan, M. Khater, F. Pagette, J. S. Rieh, D. Angell, H. Chen, J. Florkey, F. Golan, D. R. Greenberg, R. Groves, S. J. Jeng, J. Johnson, E. Mengistu, K. T. Schonenberg, C. M. Schnabel, P. Smith, A. Stricker, D. Ahlgren, G. Freeman, K. Stein, and S. Subbanna, "Self-aligned SiGe NPN transistors with 285 GHz f_{MAX} and 207 GHz f_T in a manufacturable technology," *IEEE Electron Device Lett.*, vol. 23, no. 5, pp. 258–260, May 2002.

[8] T. Vanhoucke and G. A. M. Hurkx, "Unified electro-thermal stability criterion for bipolar transistors," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meet.*, 2005, pp. 37–40.

[9] T. Vanhoucke, H. M. Boots, and W. D. van Noort, "Revised method for extraction of the thermal resistance applied to bulk and SOI SiGe HBTs," *IEEE Electron Device Lett.*, vol. 25, no. 3, pp. 150–152, Mar. 2004.

[10] C. Hu, S. C. Tam, F. C. Hsu, P. K. Ko, T. Y. Chan, and K. W. Terrill, "Hot electron induced MOSFET degradation—Model, monitor, and improvement," *IEEE Trans. Electron Devices*, vol. 32, no. 2, pp. 375–385, Feb. 1985.

[11] D. J. DiMaria and J. W. Stasiak, "Trap creation in SiO_2 produced by hot electrons," *J. Appl. Phys.*, vol. 65, pp. 2342–2356, Mar. 1989.

[12] K. L. Brower, "Kinetics of H_2 passivation of P_b centers at the (111) Si-SiO_2 interface," *Phys. Rev. B*, vol. 38, pp. 9657–9666, Nov. 1988.

[13] L. Tsetseris, R. D. Schrimpf, D. M. Fleetwood, R. L. Pease, and S. T. Pantelides, "Common origin for enhanced low-dose-rate sensitivity and bias temperature instability under negative bias," *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, pp. 2265–2271, Dec. 2005.

[14] L. Tsetseris, X. J. Zhou, D. M. Fleetwood, R. D. Schrimpf, and S. T. Pantelides, "Physical mechanisms of negative-bias temperature instability," *Appl. Phys. Lett.*, vol. 86, p. 142103, 2005.

[15] D. M. Fleetwood, F. V. Thome, S. S. Tsao, P. V. Dressendorfer, V. J. Dandini, and J. R. Schwank, "High-temperature SOI electronics for space nuclear power systems: Requirements and feasibility," *IEEE Trans. Nucl. Sci.*, vol. 35, no. 5, pp. 1099–1113, Oct. 1988.

[16] M. R. Shaneyfelt, J. R. Schwank, D. M. Fleetwood, R. L. Pease, J. A. Felix, P. E. Dodd, and M. C. Maher, "Annealing behavior of linear bipolar devices with enhanced low-dose-rate sensitivity," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3172–3177, Dec. 2004.

[17] K. O. Jeppson and C. M. Svensson, "Negative bias stress of MOS devices at high electric fields and degradation of NMOS devices," *J. Appl. Phys.*, vol. 48, no. 5, pp. 2004–2014, 1977.

[18] F. B. McLean, "A framework for understanding radiation-induced interface states in SiO_2 MOS structures," *IEEE Trans. Nucl. Sci.*, vol. 27, no. 6, pp. 1651–1657, Dec. 1980.

[19] N. S. Saks and D. B. Brown, "Interface trap formation via the two-stage H+ process," *IEEE Trans. Nucl. Sci.*, vol. 36, no. 6, pp. 1848–1857, Dec. 1989.

[20] M. R. Shaneyfelt, J. R. Schwank, D. M. Fleetwood, P. S. Winokur, K. L. Hughes, and F. W. Sexton, "Field dependence of interface-trap buildup in polysilicon and metal gate MOS devices," *IEEE Trans. Nucl. Sci.*, vol. 37, no. 6, pp. 1632–1640, Dec. 1990.

[21] S. L. Kosier, A. Wei, R. D. Schrimpf, D. M. Fleetwood, M. D. DeLaus, R. L. Pease, and W. E. Combs, "Physically based comparison of hot-carrier-induced and ionizing-radiation-induced degradation in BJTs," *IEEE Trans. Electron Devices*, vol. 42, no. 3, pp. 436–444, Mar. 1995.

[22] R. L. Pease, S. L. Kosier, R. D. Schrimpf, W. E. Combs, M. Davey, M. DeLaus, and D. M. Fleetwood, "Comparison of hot-carrier and radiation induced increases in base current in bipolar transistors," *IEEE Trans. Nucl. Sci.*, vol. 41, no. 6, pp. 2567–2573, Dec. 1994.

[23] A. P. G. Prakash, A. K. Sutton, R. M. Diestelhorst, G. Espinel, J. Andrews, B. Jun, J. D. Cressler, P. W. Marshall, and C. J. Marshall, "The effects of irradiation temperature on the proton response of SiGe HBTs," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3175–3181, Dec. 2006.